ISSN: 2350-0328

International Journal of Advanced Research in Science, Engineering and Technology

Vol. 2, Issue 7 , July 2015

Optimal Choice of Using PN Code For a DDS Transmitter

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ABSTRACT: Frequency Hopping Spread Spectrum (FHSS) is a technique that wireless devices communicate such that the transmission frequencies are alternated in a pre-determined ordered hopping pattern. In tradition, the hopping sequence is controlled by using a pseudo-random code sequence (PN code) known only to both transmitter and receiver. In this paper, the carrier frequency of the Telemetry transmitter involved in this paper is interfered by the surrounding environment. Thus, FHSS will be used instead to switch between multiple carriers within the available bandwidth to minimize the interference. Such a system requires that the generated PN code ensures that all carrier frequencies within the hopping pattern should be semi-equally used during transmission. Several simulation scenarios were carried out to compare between a single Long PN code and an Accumulated Short PN code. Finally, the developed FH system is implemented using an AD9910 Direct Digital Synthesizer (DDS) and an ALTERA Cyclone-III FPGA chip.Results proved that, according to the system requirements, an Accumulated Short PN code offers noticeable residual correlations and provides a higher level of autocorrelation compared to a single Long PN code. Results, also, verified that the developed FH system using PSK provides lower Bit Error Rate (BER) than the single carrier FSK one. Section (I) is introduce the transmitter involved in the paper and its usage in the telemetry system and the problems affected on the telemetry. Section (II) shows the benefits of using DDS. Section (III) illustrates the simulation process to generate the PN code used in the frequency hopping system and make detailed and illustrated comparison between using long or accumulated short PN code. Section (IV) demonstrates the modification of the old transmitter to work as a frequency hopping system by adding a new FPGA kit to the old transmitter and reprogramming of the DDS chip. Section (V) is the conclusion of the paper.

KEYWORDS: FHSS, Telemetry, PN Code, DDS, FPGA.

I. INTRODUCTION

The signal of the transmitter of the telemetry system involves in this paper is subjected to a lot of problems affected on its performance due to the surround environment. Noise, interference, jamming etc. is represented the main environmental problems affected on the transmission. Most of the received data from the telemetry transmitter is being lost during the transmission operation due to the reasons we narrate. The main objective of this paper is to change the operation technique of the transmission from using a single carrier frequency to the transmission using multi-carrier system, using Frequency Hopping Spread Spectrum FHSS Technique, trying to improve the transmission efficiency and receiving most of the transmitted data. Frequency Hopping Spread Spectrum (FHSS) is the technique of using a multi-carrier frequency that the carrier is move from frequency to another one, within the band, randomly and fast so that we use this technique trying to upgrade the involved system from using a single frequency to use a multi-frequency system and achieving our target to eliminate the transmission problem. The paper also discuss how to choose the appropriate Pseudo Noise Code (PN code) to carry out the best hop sequence used during the transmission operation without concentration on a specific carrier from the hopped frequency band. In order to meet this objective, several phases and procedures were executed through this paper, the first phase is the software implementation, using MATLAB and FPGA Model Sim simulation and also simulate the appropriate PN Code used in the system. The system was carried out and the output is tested in the lab

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II. . DIRECT DIGITAL SYNTHESIS (DDS)

Direct digital synthesis (DDS) is a method of producing an analog waveform usually a sine wave by generating a time-varying signal in digital form and then performing a digital-to-analog conversion. Because operations within a DDS device are primarily digital it can offer fast switching between output frequencies, fine frequency resolution, and operation over a broad spectrum of frequencies. With advances in design and process technology, today's DDS devices are very compact and draw little power. Figure 1 shows a DDS chip

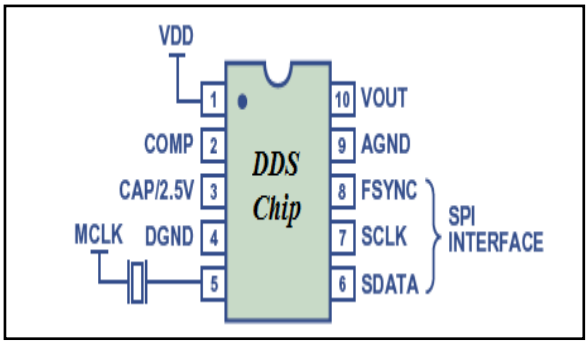

Fig.1. DDS chip

A. The main benefits of using a DDS

DDS are programmed through a high speed serial peripheral-interface (SPI), and need only an external clock to generate simple sine waves. DDS devices are now available that can generate frequencies from less than 1 Hz up to 400 MHz (based on a 1-GHz clock). The benefits of their low power, low cost, and single small package, combined with their inherent excellent performance and the ability to digitally program (and re-program) the output waveform, make DDS devices an extremely attractive solution—preferable to less-flexible solutions comprising aggregations of discrete elements. The ability to accurately produce and control waveforms of various frequencies and profiles has become a key requirement common to a number of industries. Whether providing agile sources of low-phase-noise variable-frequencies with good spurious performance for communications, or simply generating a frequency stimulus in industrial or biomedical test equipment applications, convenience, compactness, and low cost are important design considerations. For example a DDS-based programmable waveform generator operating at 5.5 V with a 25-MHz clock, consumes a maximum power of 30 mW

III.SIMULATION

In the simulation process it, we have two phases, the 1st phase is the using of MATLAB simulation tools to simulate and compare between the two PN codes (the Long PN Code and the Accumulated Short PN Code). The 2nd phase is the using the simulation tools of the FPGA ModelSim to simulate the new hardware which added to the system to operate with frequency hopping instead of the single carrier process.

A. The System Requirements:

The next table (**Table 1)** Shows the system requirements and shows the calculation needed for the length of the PN code required for the system operation.

Table 1: system requirements

The whole Test period	**3 min.**
The frame length	**10 m Sec.**
The Number of frames/sec is = 1 / (10 × 10-3)	**100 frame/sec.**
The total number of frames in the whole test = (3 min. × 60 sec. × 100 frame/ sec)	**18000 frame**

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In the system involved we use the Slow FH each frame represented by (one Hop) the total hop numbers is = the number of frames	**18000 hopset**
In the system involved we use 8 carrier frequencies. So we read the PN code by 3 digits it means that each 3 digit represent (one hop or one carrier) The PN code length required for the test is $\geq 3 \times$ 18000	**≥ 54000 bit**

First we generate the PN code using the Linear Feedback Shift Register LFSR circuit shown in Figure4 andFigure 5 for the system, then according to the number of the frequency carriers we generate a LUT and read the PN code. In the system involved we read the PN code by 3-digit and compare with LUT and then selecting the frequency hop carrier will be used at this moment as shown in Figure 2.

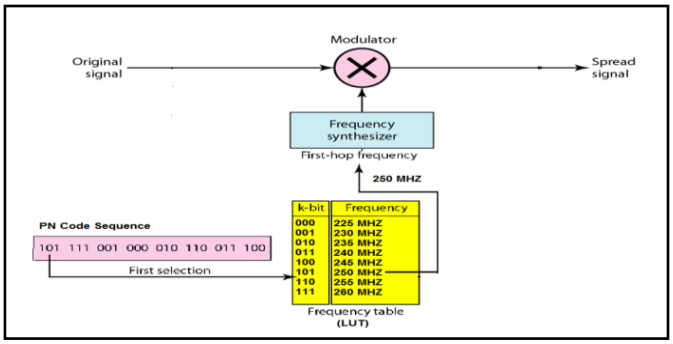

Fig.2. the hop selection in FHSS system

B. Calculation of the PN code length

We have two ways for generating a PN code of length ≥ 54000 bit. We will simulate and choose the best output result.
The 1st way is: A generation of (*long PN code sequence)*
(The traditional technique)
The 2nd way is: A generation of (*Accumulated short PN code sequence)*
Figure 3 illustrates the two ways which will compare and select the optimal output PN code and optimal output hop-set.

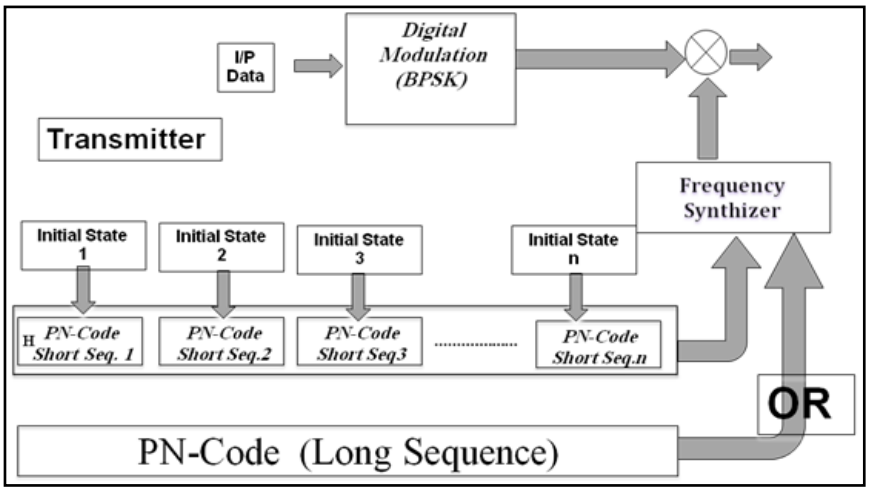

Fig.3. shows two ways to use PN code sequence in the hopping sequence

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(1) **A generation of Long PN Code Sequence (Traditional way)**

$2^n - 1 \geq 54000$

$n \ln 2 = \ln (54000-1)$

$n \geq 15.72$ so that n=16

The PN code length N = 216 -1 = 65535 bits.

So that we will use a generating polynomial of order (16) choosing it from the table in Figure 6 of the max length of PN code sequence.

Table 2 :the generating polynomial of the maximum length

n	$N=2^{n-1}$	Feedback Taps for m-sequences
2	3	[2,1]
3	7	[3,1]
4	15	[4,1]
5	31	[5,3] [5,4,3,2] [5,4,2,1]
6	63	[6,1] [6,5,2,1] [6,5,3,2]
7	127	[7,1] [7,3] [7,3,2,1] [7,4,3,2] [7,6,4,2] [7,6,3,1] [7,6,5,2] [7,6,5,4,2,1] [7,5,4,3,2,1]
8	255	[8,4,3,2] [8,6,5,3] [8,6,5,2] [8,5,3,1] [8,6,5,1] [8,7,6,1] [8,7,6,5,2,1] [8,6,4,3,2,1]

n	$N=2^{n-1}$	Feedback Taps for m-sequences
9	511	[9,4] [9,6,4,3] [9,8,5,4] [9,8,4,1] [9,5,3,2] [9,8,6,5] [9,8,7,2] [9,6,5,4,2,1] [9,7,6,4,3,1] [9,8,7,6,5,3]
10	1023	[10,3] [10,8,3,2] [10,4,3,1] [10,8,5,1] [10,8,5,4] [10,9,4,1] [10,8,4,3] [10,5,3,2] [10,5,2,1] [10,9,4,2] [10,6,5,3,2,1] [10,9,8,6,3,2] [10,9,7,6,4,1] [10,7,6,4,2,1] [10,9,8,7,6,5,4,3] [10,8,7,6,5,4,3,1]

Figure 4 shows the circuit diagram of the LFSR circuit using for generation of the Long PN code

It contents of (16) shift registers and (4) XOR logic gate for representing the 4-taps feedback.

$$g(x) = (X^{16} + X^{15} + X^{13} + X^4 + 1)$$

(2) A generation of Accumulated short PN code sequence

Using a generating polynomial of order (8) and running the LFSR circuit 255 times (all available initial states) each time we use a different initial state .So that the total PN code length is

$= (28-1) \times 255 = 255 \times 255 = 65025$ bits.

$$g(x) = (X8 + X4 + X3 + X2 + 1)$$

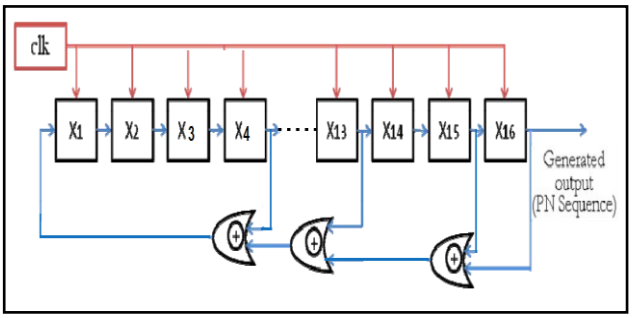

Fig.4. Circuit Diagram of 16- Bit LFSR with m- length Feedback Polynomial

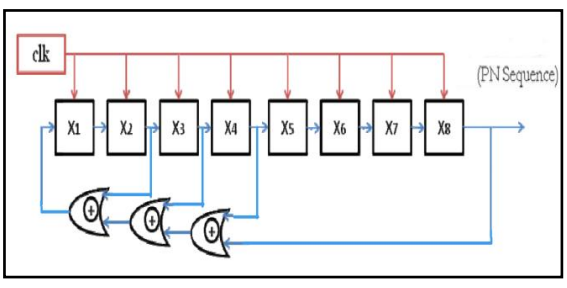

Fig.5. Circuit Diagram of 8- Bit LFSR with m- length Feedback Polynomial

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In table 3 we illustrate the comparison between the used parameters by the two ways.

Table 3: Comparison between the two ways

	Long PN Code (Tradition Way)	**Accumulated Short PN Code**
Polynomial g(x) Order Used	16	8
The PN code Length	65535 216 -1	65025 255×255
Polynomial g(x) Used	[16,15,13,4]	[8,4,3,2]
Number of taps	4 – taps	4 –taps
Number of initial states	1 initial state	255 initial state
Number of hops	21845	21675

C .The Proposed Generating PN-Code.

We will compare between the histogram of the generated Hop Sequence from Both the Long sequence and the accumulated short-sequence. The target of this system is to generate a PN code sequence controls the hopping sequence semi-equally used during transmission to ensure that none of them possess a large hopped times which may become the affected one in that test environment.
Using the parameters calculated in the table 3. And writing a MATLAB m-file and simulate the tabulated data on both the two parameters (long PN code) and (short PN code). Figure, shows the simulation results of the histogram of both long and short code

Fig. 6. Illustrates the output histogram for the(Long PN code sequence).

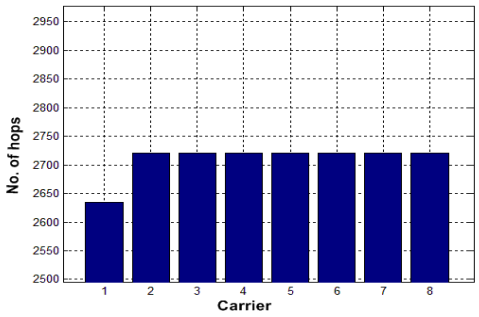

Fig.7.illustrates the output histogram for the (Accumulated short PN code sequence).

The histogram analysis conducted for the two generated hopping sequences, is depicted in Figure 6, 7 From which it can be concluded that the Accumulated short PN code sequence selection mechanism can provide better uniform distribution of frequency channels over available band better than that provided by the Long one (the Accumulated Short PN is represented by the blue colour and the Long PN is represented by the red colour).The randomness of the (Accumulated short PN code sequence) and the (Long PN code sequence) can also be verified by the auto-correlation

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Of each histogram. Figure shows the auto-correlation properties of sort sequences and long sequences. So that we compare between the autocorrelation of the both histogram result so that the next figure shows the difference between the both autocorrelation

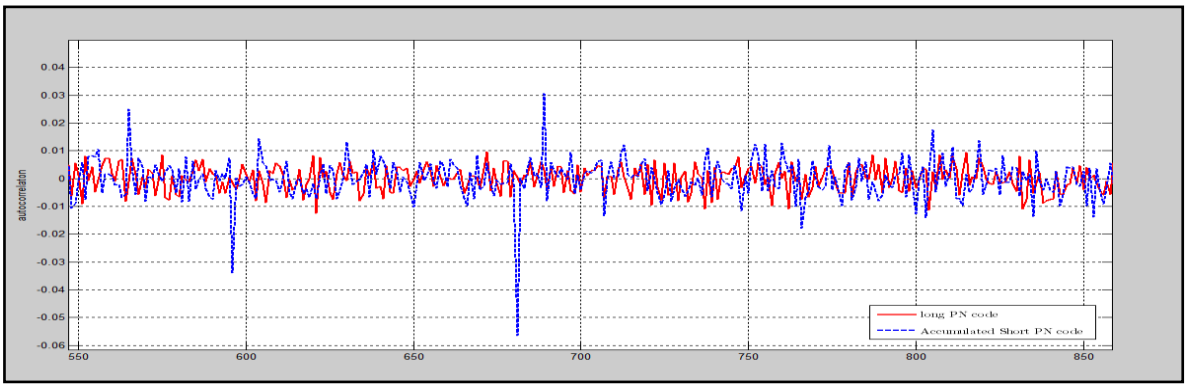

Fig.8. shows the autocorrelation between Long and Acc. Short PN code

Carrying out the simulation of obtaining the histogram and the output autocorrelation of another two systems having a PN code length of 4095 and 16383 using caparison between g(x) of order (6,12) in the 1st system and between g(x) of order (7,14) of the 2nd system.

Figures 9, 10, 11, 12, 13and 14 shows the histogram and autocorrelation of the both system which related to the same conclusion that the Accumulated Short PN code system is much better than the Long PN code.

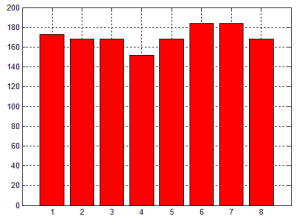

Fig.9. histogram of the 1st long PN code seq.

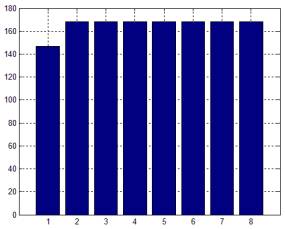

Fig.10. histogram of the 1st short PN code seq.

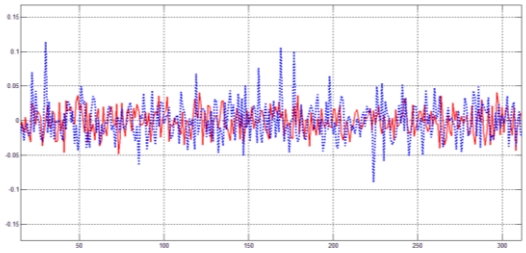

Fig.11. output autocorrelation of the 1st long and short PN code seq.

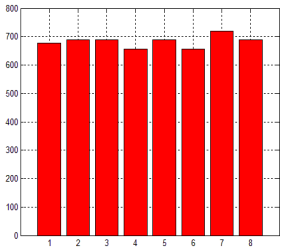

Fig.12. histogram of the 2nd long PN code seq.

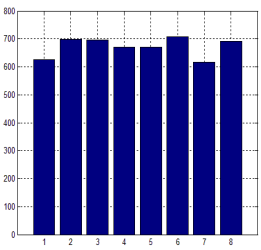

Fig.13.histogram of the 2nd short PN code seq.

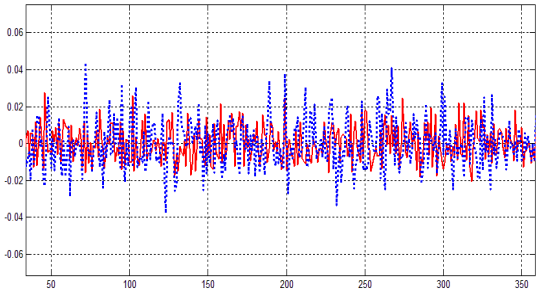

Fig.14.output autocorrelation of the 2nd long and short PN code seq.

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IV. HARDWARE IMPLEMENTATION

We will upgrade the old system involved in this paper to work as a frequency hopping system instead of single carrier one so that we will make some changes to the hardware such that we will adding a new ALTERA FPGA kit to the hardware.

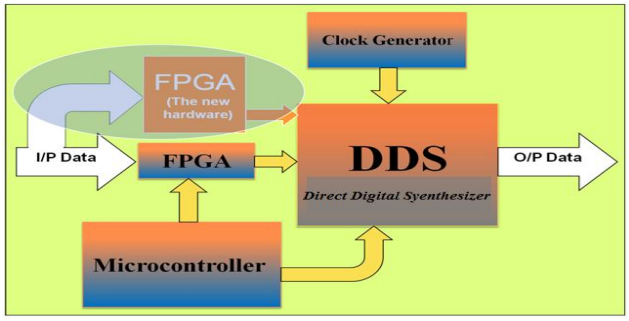

Fig.15. block diagram of the Transmitter upgrade

A. Synchronization of the frame with the DDS

In the Transmitter involves we use the slow frequency hopping technique its mean that every transmitted frame will transmitted via independent hop carrier, moreover upgrading the system needs a synchronization between the transmitted frames with output hop carrier. The system requires an indication to the DDS chip to synch between the frame and the output hop carrier.

Figure 16 shows the output pulse which will trigger the DDS for the new hop carrier.

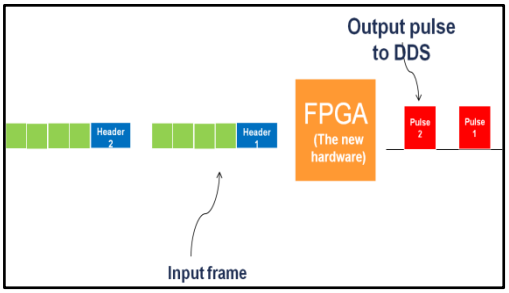

Fig.16. the function of the new FPGA

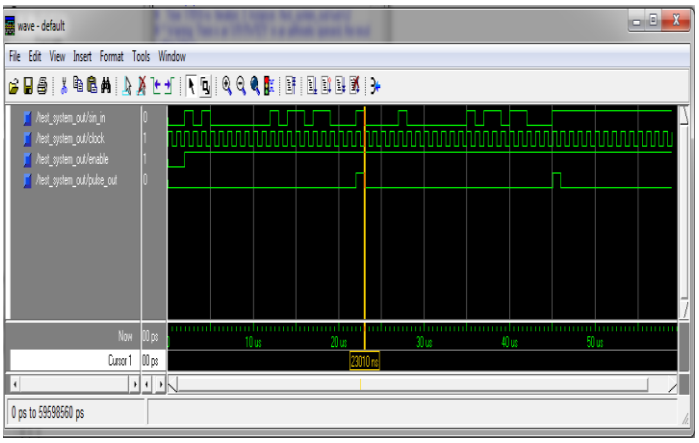

Fig.17. the VHDL simulation output of the pulse using for synchronization.

The usage of FPGA kit and designing VHDL code give an output pulse indication to the DDS to control the output carrier for each input frame to the system.

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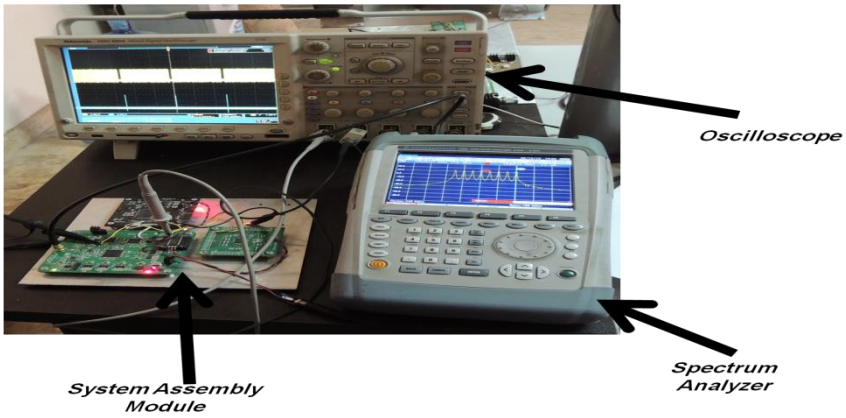

Fig.18.shows the instrumentation set up for the hardware

V. CONCLUSION

From the system involved we conclude that the usage of (Accumulated Short PN Code sequence) is much better that using a (Long PN Code sequence) in the generation of the hopping sequence for achieving frequency hopping sequence pattern of carriers should be semi-equally used during transmission. Moreover the output of the histogram and the results of the autocorrelation of each code show the best PN code.

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