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High Throughput Redundant Binary Technique for Partial Product Generation

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ABSTRACT: High modularity and carry-free addition can be used by the Redundant Binary (RB) method. In conventional method an additional error correcting word (ECW) is generated in RB multiplier. it requires in both RB multiplier and radix-4 (MBE) modified booth encoding. The number of accumulation stages are increases, in order to reduce the number of stages proposed (RBMPPG) redundant binary modified partial product generation method can be introduced. An extra Error Correcting Word (ECW) is removed and saves a one accumulation stages. The proposed RBMPPG generates fewer partial product rows than conventional RB MBE multiplier. The proposed RB MBE method simulation results shows significantly improves the area and delay for the word length of each operand in the multiplier is at least 8bits. Compared with existing RB multiplier the proposed (RBMPPG) reduces the area delay product up to 50 percent compared with existing RB multipliers.

KEYWORDS: Redundant binary, modified booth encoding, RB partial product generator, RB multiplier.

I. INTRODUCTION

The arithmetic units of Microprocessor, multimedia, and digital signal processors are applied in digital multipliers. To design a high speed and low power multipliers many algorithm and architectures are proposed. There are three steps to include the Normal Binary (NB) multiplication by digital circuits. First step generation of partial product, second step to remain two partial product rows all partial products are added by partial product reduction tree. In third step, the fast carry propagation adder can be added by using two partial product rows. To perform a partial product reduction two methods can used. The four-two compressors are used in a first method. The Redundant Binary (RB) numbers are used in a second method. The partial product reduction tree can be reduced and can be used for both methods.

To perform signed-digit arithmetic the redundant binary number representation has been introduced by avizienis [1]. The capability of RB number can be represented in different ways. By using redundant binary addition trees the fast multipliers can be designed [6].Floating point processor and redundant binary representation are implemented in VLSI[5].Due to advantageous features, high performance of RB multipliers become popular such as high modularity and carry-free addition [8].

To reduce the number of partial product rows by half the radix-4 booth encoding is modified and used in partial product generator for both booth and MBE multipliers in parallel multipliers. In both RB and booth encoding an additional ECW is required.

$$NRBPPAS= [\log_2(N/4+1)]$$
$$= n-1, \text{if } N=2^n \qquad (1)$$

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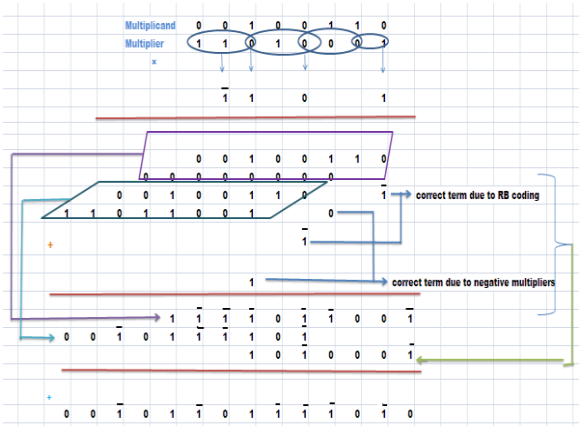

Fig.1. Conventional 8 bit NBBE multiplier

II. ANALYSIS OF BOOTH ENCODING AND RB PARTIAL PRODUCT GENERATOR

A. RADIX-4 BOOTH ENCODING

Booth encoding is used to facilitate the two's complement multiplication of binary numbers. The sets of three adjacent bits are formed in the multiplier bits. In neighboring groups the two side bits are overlapped in which it is {b1,b0,0}. The decoded partial product are selected by a each group. And 2A from the table1 shows the twice the value of multiplicand, it can be performed by left shifting. Each bit of A and adding '1' the negation operation can be obtained. For RB MBE multipliers the problem cannot be solved.Radix-4 booth encoding is used to solve the problem in correcting bits for multiplier of (NBBE-2) multipliers. By inverting each bit of A and adding '1'the negation operation is achieved. The encoder and decoder operations are used in a partial product reduction tree.

TABLE 1
Scheme of MBE

b2i+1,b2i, b2i-1	operation
000	0
001	+A
010	+A
011	+2A
100	-2A
101	-A
110	-A
111	0

B. RB PARTIAL PRODUCT GENERATOR

RBPP is generated from two NB partial products, one RB digit is used to represent by two bits. Using two's complement representation the addition of two N-bit partial products X and Y are used. Adding -1 from the NB partial product to the LSB and RBPP is generated. The errors are introduced in both the MBE and RB coding. 1) -1 must be added to the LSB of RB number when RB format is converted by a NB number. 2) During the booth encoding the

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multiplicand is multiplied by -1 or -2. From both the radix-4 and RB encoding a single ECW can compensate the errors. The N/4 RBPP rows and one ECW included by a N-bit CRBBE-2.

$$ECW = E\left(N/4\right)0\ F\left(N/4\right)0 \ldots .0E_{i2}0F_{i0} \ldots 0E_{i2}0F_{10} \quad (2)$$

Where i represents the i[th] row in the RBPP's. Booth encoding is determined by using the error correcting digit.

$$Ei_2 = \begin{cases} 0, no\ negative\ encoding \\ 1, negative\ encoding \end{cases}$$

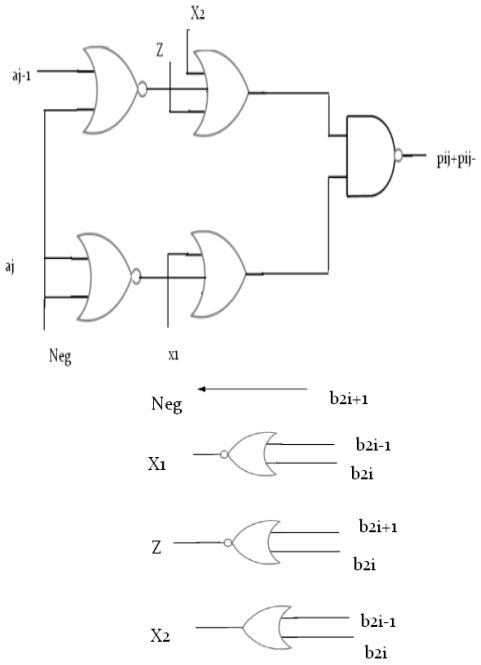

Fig.2. MBE scheme of encoder and decoder

An encoder accepts an active level on one of its input level representing digit such as decimal or octal digits and converted in to coded output such as BCD or Binary. Decoder is a logic circuit that accepts a set of inputs that represents the binary number and activates only the output that corresponds to input number.

TABLE 2
RB Encoding

X_i^+	X_i^-	RB digit(X_i)
0	0	0
0	1	$\bar{1}$
1	0	1
1	1	0

III. METHOD OF PROPOSED RB PARTIAL PRODUCT GENERATOR

In this method error correction is eliminated using new RB modified partial product generator and partial product rows are reduced from 3 to 2 stages.

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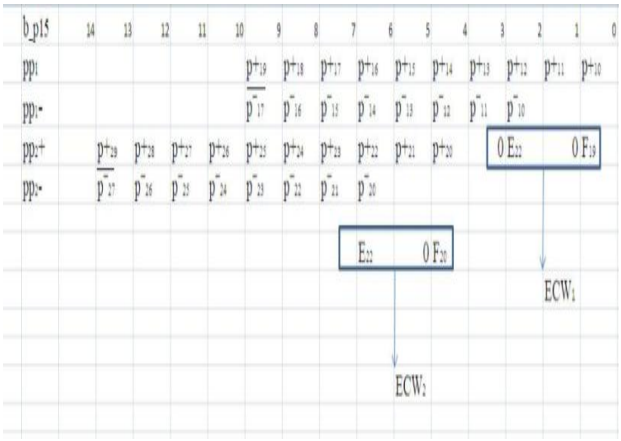
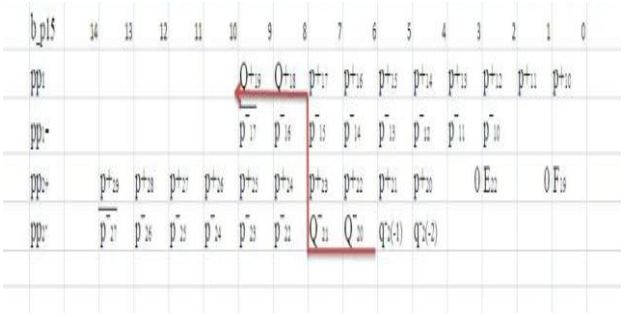


(a)

Fig.3.(a) 8-bit MBE multiplier of a new RBMPPG architecture.

By using Booth multiplication and redundant Binary Multiplier the values are to be calculated and shown in Fig.3.(a) The Error Correcting Word (ECW) is generated



(b)

Fig.3.(b) Proposed RBMPPG-2 architecture eliminating ECW_2.

The error correcting words are combined in free space of partial product terms and shown in Fig.3.(b) and by combining the number of accumulation stages.

$$ECW_1 = 0E_{12}\,0F_{10} \qquad (3)$$

By using PP_1 the ECW_1 is generated.

$$ECW_2 = 0\,E_{22}\,0\,F_{20} \qquad (4)$$

PP_1 and PP_2 are to be combined with ECW_2 to eliminate the RBPP accumulation stages. The first (PP_1^+) MSB of first partial product row and $(PP_{N/4}^-)$ last partial product of two LSB_s of last partial product row are eliminated using Error Correction Word (ECW). The area and delay product can be reduced.

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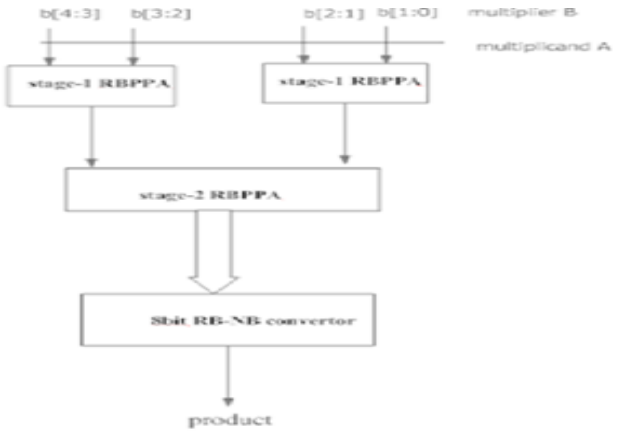

Fig.4 Block diagram of 8-bit RB multiplier

The Multiplicand A is Multiplied with a Multiplier B. the partial product terms are generated in a Stage-1 RBPPA and shown in Fig.4. the 8 bit values are combined in a stage-2 RBPPA to convert a Redundant Binary to Normal Binary convertor. Finally the product term is generated.

A. Proposed RBMPPG-2

The pp1 and pp2 are incorporated to eliminate the RBPP accumulation stages. The area delay process can be reduced. Than other gates the two input NAND gate and Transmission gate (TG) are faster.

By generating Q_{18}^{+},Q_{19}^{+},Q_{20}^{+},Q_{21}^{+} the delay of RBMPPG-2 is reduced. Whereas Q_{18}^{+} shows a longest path delay.

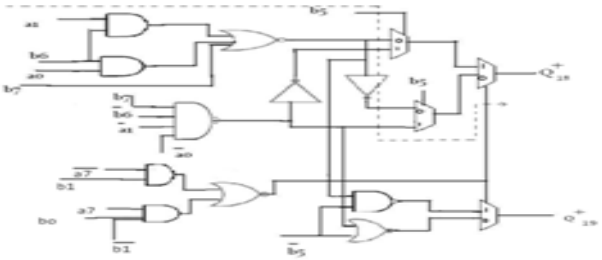

Fig.5. Modified partial product variables $Q_{18}^{+}$and Q_{19}^{+}.

In normal booth multiplier the accumulation stages will not be reduced and number of partial products remains the same. The invertors are connected in a Mux shown in a Fig.5.

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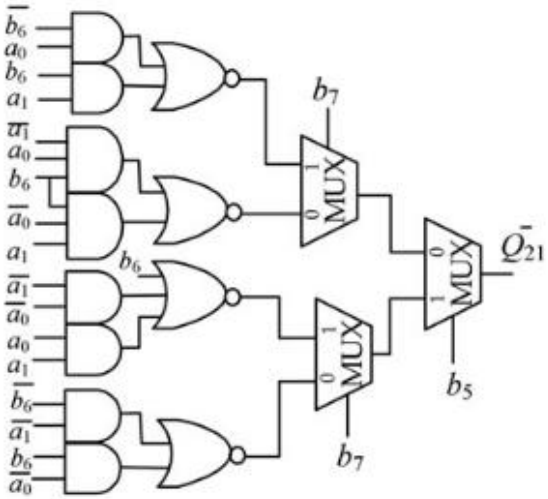

Fig.6. Modified partial product variables Q^{-}_{21}.

By eliminating the invertors from mux the number of stages can be reduces easily.

$$Q_{18}^{+} = (b_7 \oplus b_5 + b_7 b_6 b_5).p_{18}^{+} + \bar{b}_7 \bar{b}_5.(\overline{p^{-}_{21} + p^{-}_{20}}) \oplus p_{18}^{+}) + b_{7\overline{b_6}} b_5 .(p^{-}_{21} p^{-}_{20} \oplus p_{18}^{+})$$

$$Q_{19}^{+} = (b_7 \oplus b_5 + b_7 b_6 b_5).p_{19}^{+} + \bar{b}_7 \bar{b}_5.\overline{(p_{18}^{+} + p^{-}_{21})} + p_{20}^{-} p_{19}^{+}) + b_{7\overline{b_6}} b_5 .(p_{18}^{+} p^{-}_{21} p^{-}_{20} \oplus p_{19}^{+})$$

$$Q_{21}^{-} = (b_7 \oplus b_5 + b_7 b_6 b_5).p_{21}^{+} + \bar{b}_7 \bar{b}_5.(\overline{p_{21}^{-} + p^{-}_{20}}) + b_7 \overline{b_6} b_5 . p_{21 \oplus}^{-} p_{20}^{-})$$

B. METHOD OF RBMPPG-2 BASED HIGH-SPEED RB MULTIPLIERS

The 2^n-bit RB multipliers can be applied in a proposed RBMPPG-2 with a reduction of a RBPP accumulation stage compared with conventional method. Therefore delays of multiplier stages are reduced. There are 3stages in proposed 8-bit RBPP accumulation stages and it is reduced from 3stages to 2 stages. Compared with conventional CRBBE-2 method 20 percent delay time is reduced in proposed RBPP method.

IV. PERFORMANCE ANALYSIS

The performance of RBMPPG is proposed using Xilinx tool. The NBBE-2, CRBBE-2 and RBBE results are compared. In final stage RB multiplier is converted into NB multiplier to form a two's complement number. The multiplier designs are introduced at gate level in verilog HDL and verified by Xilinx. In Table 3. The area and delay are to be shown using the covalent redundant binary booth encoding (CRBBE) and redundant binary booth multiplier. Compared with existing covalent redundant binary booth encoding the proposed redundant binary booth multiplier is more efficient.

TABLE 3
Design Results of CRBBE and RBBE multipliers using Xilinx ISE Tool

Techniques	Area in slices	Area in LUT_s	Delay(ns)
Normal Binary Booth Encoding Multiplier(NBBE)	320	840	21.2

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Covalent Redundant Binary Booth Encoding(CRBBE)	281	725	14
Redundant Binary Booth Multiplier	233	600	3.2

V. CONCLUSION

In this paper, a new modified RBPP generator method is proposed. In previous stage the additional ECW (Error Correction Word) is introduced. Due to elimination of ECW the RBPP accumulation stage is saved. To reduce the number of RBPP rows from N/4+1 to N/4 the RB partial product generation technique can be applied to any 2^n-bit RB multipliers. The performance of RB MBE multipliers using the proposed RBMPPG-2 is improved and shown in simulation results. The area delay product can be reduced more than 50percent using proposed RB multipliers. Hence, designing area delay efficient power of two RBMBE multipliers is very useful technique using proposed RBPP generation method. The proposed RBPP are to be applied in image processing.

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