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An Efficient Design of Dadda Multiplier Using Compression Techniques

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ABSTRACT: In Digital Signal processing, data compression is a widely used technique which primarily focuses on multimedia and image processing applications by delivering the information/data in a compact size. Approximate computing is one of the interesting paradigm in arithmetic designs. The main objective of the approximate design is to reduce the power, area and delay. This paper proposes four different compression schemes that are analyzed for a 8X8 Dadda multiplier and its application on image processing where pixel by pixel multiplication is been carried out. The result shows that there is a significant reduction in power, area and delay when compared to the existing design; also the proposed designs show excellent capabilities for image multiplication in terms of Peak Signal to Noise Ratio (PSNR).

KEYWORDS: Dadda Multiplier, 4:2 compressor, Approximate design, Peak-to-Signal Noise Ratio(PSNR).

I. INTRODUCTION

The digital logic circuits which operate with high degree of reliability and precision are used to implement many arithmetic applications. Several image and video processing algorithms are implemented by these digital circuits and for human visibility it seems to be accurate though it remains numerically approximate. The numerical accuracy relaxation provides some freedom to carry out approximate computation. This idea provides low-power designs with less area and delay in different abstraction levels. Approximate and probabilistic adders determined by its figure of merit for inexact computing are been compared using several adders and new metrics by Liang et al.[10].

Error Distance (ED) is a parameter in image processing which is described as the difference between the actual output and an error output for a given input [10]. Peak Signal-To-Noise Ratio often abbreviated PSNR is used to determine the quality of reconstruction of lossy compression codecs (e.g., for image compression).PSNR is an approximation to human perception of reconstruction quality and easily defined via the Mean Squared Error (MSE).

This paper is organized as follows: Chapter 2 explains the survey of different multipliers in existence. Chapter 3 gives the detailed description of exact 4:2 compressors. Chapter 4 presents the proposed approximate 4:2 compressors. Chapter 5 deals with the implementation of approximate compressors in Dadda multiplier. In Chapter 6, results and discussions are clearly manifested. Finally, Chapter 7 concludes the paper.

II. SURVEY OF DIFFERENT MULTIPLIERS

Multiplication plays a major role in digital signal processing. In fact it is the most commonly used operation in various processes. Parallel multipliers are a high speed multiplier which requires high area implementation. Therefore it is not an effective multiplication method. On the other hand, Truncated multiplier multiplies the data by adding the most significant columns of the multiplication matrix, along with a correction constant term[13].It achieves low area consumption of rounded output multipliers. Various signal processing algorithms and architectures are in need of low power designs for multimedia devices.

Fast multiplier design widely uses compressors in order to speed up the partial product reduction tree and to reduce the power dissipation[5],[11]. Optimized 4-2 compressors have been proposed in [3],[5],[6],[12].In neural network applications, an imprecise array multiplier[10] has been used by omitting few of the least significant bits in the partial products(hence by removing some adders in the array).An approximate multi-bit adder cell is designed using imprecise or approximate full adder with reduced circuit complexity at transistor level. It produces 17 incorrect results out of 32 states and thus it becomes inefficient.

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III. EXACT 4:2 COMPRESSOR DESIGN

In the multiplication process, compressors are normally used to serve two major purposes, (i) to speed up the operation (ii) to reduce the number of stages in the partial product generation. The main goal of this exact compressor is to provide an accurate output but with high power consumption, area and delay. Basically 4:2 compressor came into existence to replace the usage of more number of full adders. The general block diagram of 4:2 compressor is shown in Fig.1. It consists of X1, X2, X3, X4 as 4 inputs with a carry in (Cin) and sum, carry as outputs with a carry out (Cout) for propagation.

$$Sum = x1 \oplus x2 \oplus x3 \oplus x4 \oplus Cin \quad (1)$$

$$Cout = (x1 \oplus x2)x3 + \overline{(x1 \oplus x2)}x1 \quad (2)$$

$$Carry(x1 \oplus x2 \oplus x3 \oplus x4)Cin + \overline{(x1 \oplus x2 \oplus x3 \oplus x4)}x4 \quad (3)$$

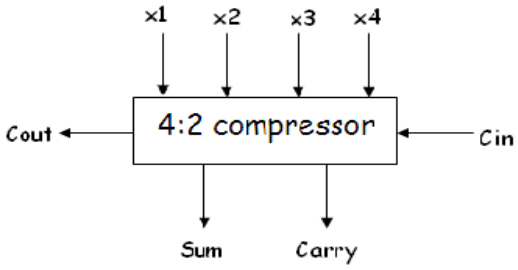

Fig 1 : Block Diagram of 4:2 compressor

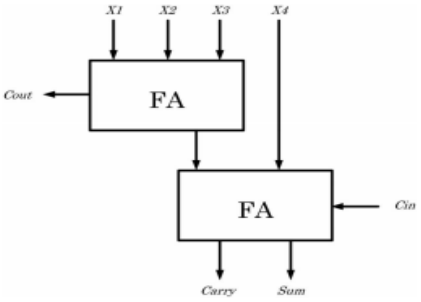

Fig 2 : Compressor using two full adders

The carry out (Cout) is a one bit binary number with higher significance whereas the four inputs and sum output carry the same weight. Since the carry in (Cin) bit acts as one of the inputs to the compressor, it will have lower significance while the output Carry out (Cout) comes with higher significance. There are two types of implementation for the exact compressor as follows:

(i)Using two Full Adders (FA).

(ii)Using XOR-XNOR module with a multiplexer.

The first method is implemented by a series of two full adders is shown in figure 2. Each will possess 3 inputs and 2 outputs. The Carry of first FA will be propagated to the next FA as Cin and thus producing Sum and carry as final outputs. The second method XOR-XNOR denoted by XOR* produces XOR and XNOR signals simultaneously which is shown in figure 3. The multiplexer will have a select line with which the input signals are chosen for output.

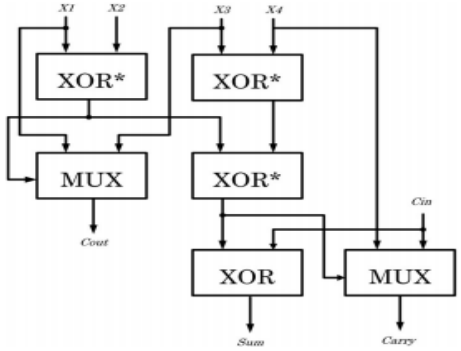

Fig 3: Optimized 4:2 compressor

IV. APPROXIMATE 4:2 COMPRESSORS

In this section, two approximate compressor designs are proposed. There were ample methods that could be substituted for approximation but they are not efficient in terms of accuracy and optimization. In [9], an approximate full adder cell has been substituted in the place of an exact full adder cell but it produces at least 17 incorrect results out of 32 possible outputs, therefore the error rate is more than 53 percent (error rate is calculated by the ratio of erroneous

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outputs to the total number of outputs).Here, two designs are proposed to reduce these errors so as to improve the performance with respect to area, power and delay.

A. DESIGN-1 APPROXIMATE COMPRESSOR

In an exact compressor, the output carry has the same value of Cin in 24 out of 32 states. While designing an approximate compressor, this feature must be considered.

$Carry = Cin$ (4)

$Sum = \overline{Cin}(\overline{x1 \oplus x2} + \overline{x3 \oplus x4})$ (5)

$Cout = \overline{\overline{x1x2}\ + \overline{x3x4}}$ (6)

In Design 1, the carry is made equal to Cin by changing the value of other eight outputs.

Table 1 : Truth table of Design1 Compressor

Cin	X4	X3	X2	X1	Cout	Carry	Sum
0	0	0	0	0	0	0	**1**
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	**0**	0	**1**
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	**1**	**0**	0
0	1	0	1	0	**1**	**0**	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	**0**	**1**
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	**0**	**1**
1	0	0	0	0	0	**1**	**0**
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	**0**	**1**	**0**
1	0	1	0	0	0	1	0
1	0	1	0	1	1	**1**	**0**
1	0	1	1	0	1	**1**	**0**
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	0
1	1	0	0	1	**1**	1	**0**
1	1	0	1	0	**1**	1	**0**
1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	**0**
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	**0**

Since the output carry gains the higher weight of a binary bit, an error value of this signal will be producing a difference value of two in the output. The substantial difference may not be acceptable but it can be compensated

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/reduced by sum and Cout simplifications. This simplification of sum to a value of 0 in the second half of Table 1 reduces the difference between exact and approximate outputs as well as the design complexity.

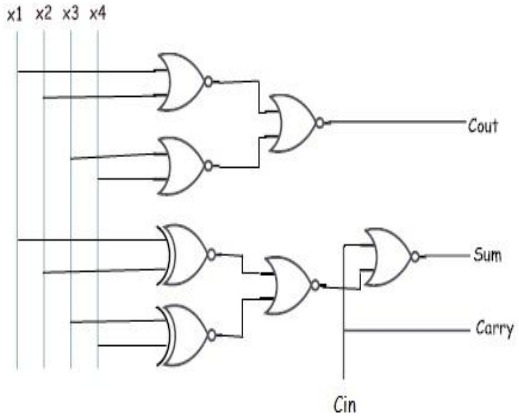

Fig 4 : Logic Diagram of Design 1 Compressor

There occurs some errors on the sum signal which will result in the reduction in the overall delay of the design (critical path). This design contains 12 incorrect outputs out of 32 outputs (error rate =37.5%) which is less than the approximate full-adder cell.

B. DESIGN-2 APPROXIMATE COMPRESSOR

Design 2 is proposed for two main reasons, to increase the performance and to reduce the error rate. The carry and Cout outputs have the same weight; therefore the equations for the carry and Cout in the previous design can be interchanged. Cin and Cout can be ignored in the hardware design since they will be zero in all stages (i.e., Cin is zero in the first stage).

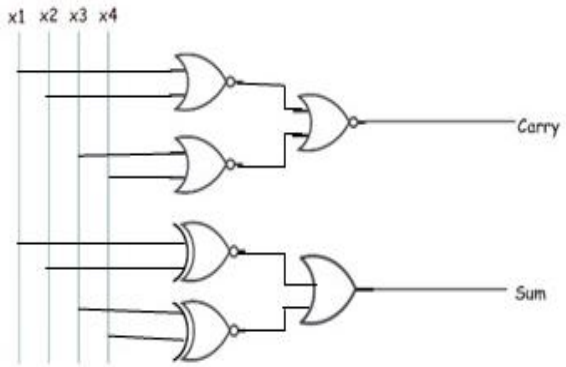

Fig 5 : Logic Diagram of Design 2 compressor

This proposed design contains 4 incorrect outputs out of 16 outputs, so its error rate has been reduced to 25 percent. This seems to be a positive approach because the amount of imprecision found to be smaller than the existing schemes.

$$Sum = \overline{x1 \oplus x2} + \overline{x3 \oplus x4} \quad (7)$$

$$Carry = \overline{\overline{x1x2} + \overline{x3x4}} \quad (8)$$

C. 3:2 COMPRESSOR

The full adders are replaced by 3:2 compressor high speed and low power consumption. It consists of XOR gates and Multiplexer so as to minimize the number of logic gates, power and delay. The functionality remains the same as the full adder but structurally different. The first two stages of multiplier uses 3:2 compressor for effective performance.

The multiplexer selects the input that has to be delivered as final carry. The sum is calculated using 2 XOR gates similar to a full adder.

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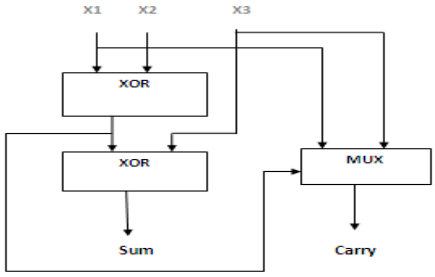

Fig 6 : Block Diagram of 3:2 Compressor

V. MULTIPLICATION

In this section, the implementation of proposed compressors on multiplier is analyzed. An exact multiplier with high speed is composed of three modules.

(i)Partial Product Generation.
(ii)A Carry Save Adder (CSA) tree for the reduction of partial products.
(iii)A Carry Propagation Adder (CPA) for final computation of result.

In a multiplier design, the second module plays a major role with respect to delay, power consumption and circuit complexity. Compressors are usually used to increase the speed of the CSA tree and decrease its power dissipation in order to achieve low-power operation. These approximate compressors lead to the design of approximate multipliers.

An unsigned 8*8 Dadda tree multiplier is chosen for the usage of proposed compressors in multipliers. Figure 5 illustrates the reduction circuit of an exact multiplier where two half-adders, two 3:2 compressors (instead of full adders) and eight 4:2 compressors are utilized in the first stage to reduce the partial products to at most four rows. In the very next stage, one half-adder, one 3:2 compressor and ten compressors are used to calculate the 2 final rows of partial products. Hence, 2 stages of reduction and 3 half adders, three 3:2 compressors and 18 compressors are needed in this reduction of 8x8 Dadda tree multiplier.

In this work, we considered four cases to design an approximate multiplier.

Case 1 – Multiplier 1 :

Design-1 4:2 compressors are used all over the stages (figure 7).Totally 3 half adders, three 3:2 compressors and 18 4:2 compressors are utilized.

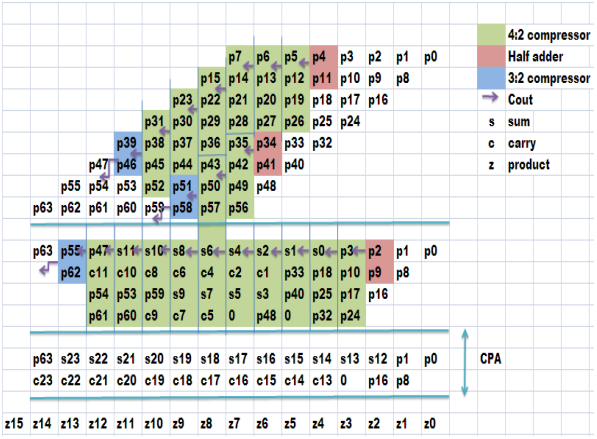

Fig 7 : Dadda Multiplier using Design-1 compressor

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Case 2 – Multiplier 2 :

Design-2 4:2 compressors are used. Less number of compressors are required for the reduction circuitry since Cin and Cout are absent (figure 8).This multiplier uses 6 half adders, one 3:2 compressor and 17 4:2 compressors.

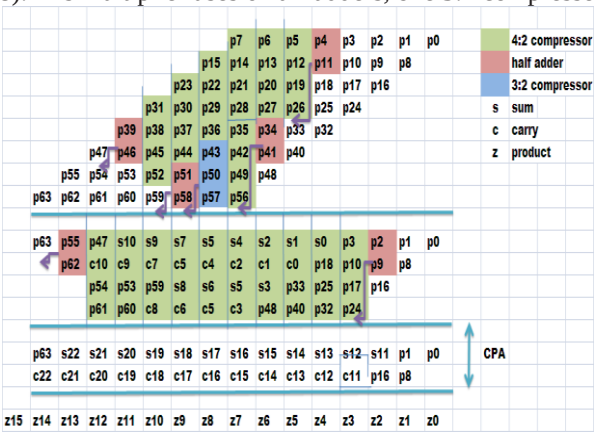

Fig 8 : Dadda Multiplier using Design-1 compressor

Case 3 – Multiplier 3 :

Two combinations are used in this case. The 'n' most significant columns in the reduction circuitry design uses exact 4:2 compressors and 'n-1' least significant columns uses Design-1 4:2 compressor. This in turn will improve the accuracy by reducing the error rate as shown in figure 9.

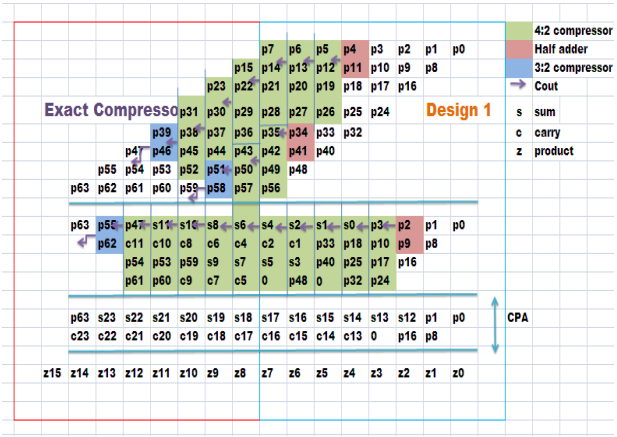

Fig 9 : Dadda Multiplier using Exact and Design-1 compressor

Case 4 – Multiplier 4 :

The 'n' most significant columns in the reduction circuitry design uses exact 4:2 compressors and 'n-1' least significant columns uses Design-2 4:2 compressor as shown in figure 10. This gives more appropriate solution when compared to the multiplier-3.

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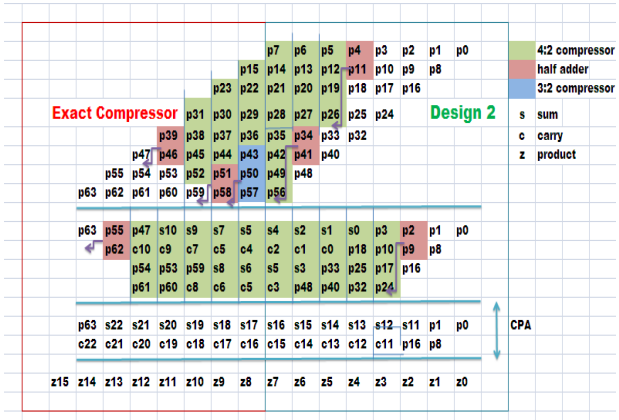

Fig 10 : Dadda Multiplier using Exact and Design-2 compressor

VI. PERFORMANCE ANALYSIS

The performance analysis is done using CADENCE and XILINX ISE tools to analyze the efficiency of the design on both ASIC and FPGA. It is found that Design-2 works more efficient in terms of power, delay and area than Design-1.For improved accuracy, Design-3 and Design-4 holds good with modest power, area consumption and delay.

A. ASIC IMPLEMENATION

In the ASIC implementation power(nW),area(cell area) and delay(ps) parameters are analysed for Exact, Design 1 and Design 2 compressors.

Table 2 : Analysis using CADENCE

PARAMETERS	DESIGNS		
	Exact	Design-1	Design-2
Power (nW)	11847.548	2537.615	1949.708
Area (Cell area)	140	77	53
Delay (ps)	848	479	306

B. FPGA IMPLEMENTATION

In the FPGA implementation power(mW),area(Number of LUTs) and delay(ns) parameters are analysed for 4 different multipliers.

Table 3 : Analysis using Xilinx ISE

DESIGNS	PARAMETERS		
	Power(mW)	Area(No. of LUTs)	Delay(ns)
Exact Multiplier	59	136	20.468
Multiplier-1	52	127	18.251
Multiplier-2	47	125	19.757
Multiplier-3	59	133	19.329
Multiplier-4	56	133	20.218

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VII. CONCLUSION

Thus the proposed approximate compressors with an implementation on Dadda multiplier has been discussed. The first and second multipliers have significant reduction on delay, area and power. The third and fourth multipliers have modest reduction with best accuracy. This proposed multipliers are to be applied on image processing to multiply two images on a pixel by pixel basis, therefore blending two images into a single image with high PSNR.

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