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Ground Bounce Noise Reduction in 4 -Bit Multiplier Using Dual Switch Power Gating Technique

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ABSTRACT: In present work, multiplier is designed using MTCMOS(Multi-Threshold CMOS) technology in 32nm length. It is simulated using HSPICE and the performance parameters such as average power, leakage current and ground bounce noise are analyzed. Obtained results are compared with other techniques and it is observed that dual switch mode power gating technique is best and comparable among all existing techniques.

KEYWORDS: dual switch mode MTCMOS technique**,** ground bounce noise, leakage current, average power

I.INTRODUCTION

The way toward scaling advancements to nano-meter administration has brought about a quick increment in spillage power scattering (static and dynamic power dispersal). Diminishing the static power scattering has turned out to be critical amid times of inertia to create outline procedures. Without exchanging off execution the power lessening must be accomplished which makes it harder to diminish spillage amid (ordinary) task at runtime. In sleep or standby mode to decrease the spillage power there are a few procedures that are utilized. Surely understood strategy is power gating system where a sleep transistor is included between virtual ground (circuit ground) and genuine ground rail. In the sleep mode to remove the spillage way, the gadget is killed. This procedure gives a considerable diminishment in spillage at a negligible effect on execution.

It has been found that the Power Gating system utilizes high threshold voltage (V_{th}) sleep transistors. At the point when the square isn't exchanging high sleep transistors are cut off VDD from a circuit piece. An essential plan parameter is size of the sleep transistor and this strategy is otherwise called MTCMOS. To accomplish long haul spillage power diminishment a remotely exchanged power supply is an extremely essential type of power gating. Power can be controlled by power gating controllers and to give power to the hardware CMOS switches are used. The power gated yields square releases gradually. Subsequently voltage levels of the yield square invest more energy in limit voltage level (V_{th}) and in this manner it prompts bigger short out current in the circuit. NMOS footer switches can likewise be utilized as sleep transistors in the plan of power gating system.

The sleep transistors can be embedded to part the chip's power organize into a perpetual power arrangement associated with the power supply and a virtual power organize that drives the cells and can be killed. By utilizing of cell-or group based approach or a circulated coarse-grained approach power gating can be actualized.

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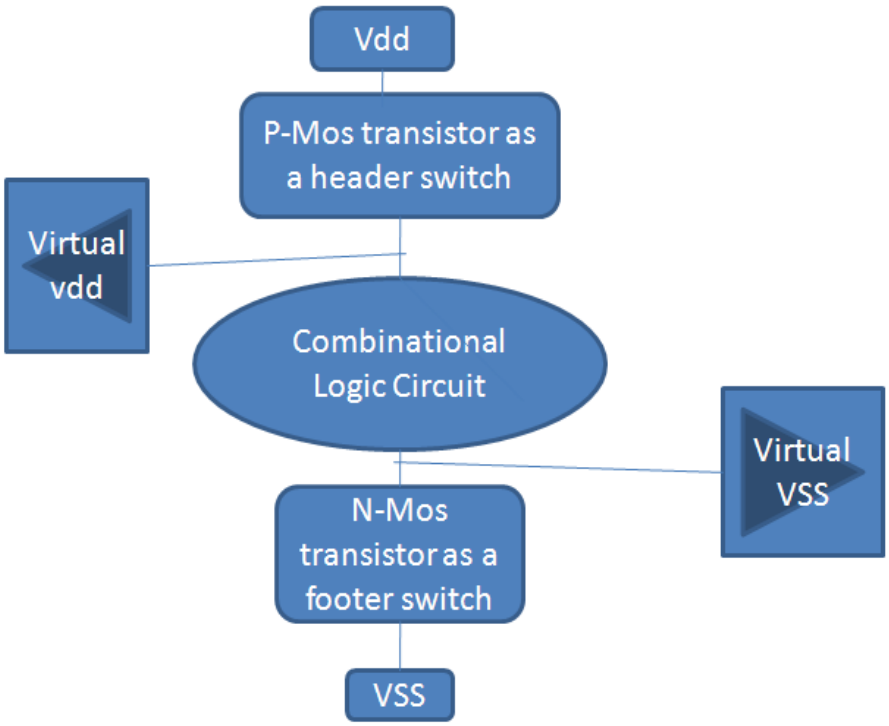

Fig.1Power gated circuit

Flag respectability is a significant issue in VLSI circuits and is winding up progressively imperative as the base component size of gadgets contracting to 130 nanometers and underneath. A noteworthy segment of the circuit commotion is the inductive clamor. Indeed, speedier clock speeds and bigger number of gadgets and I/O drivers as directed by Moore's Law (and hence bigger estimation of aggregate circuit current) have brought about expanded measure of this sort of clamor in the power and ground planes (i.e., the commotion, otherwise called the power/ground bob). It is a basic and testing configuration assignment to control the measure of inductive commotion that is embedded into the power planes. Bundle pins, holding wires, and on-chip IC interconnects all have parasitic inductances. At the point when an inductor current encounters time-area variety, a voltage vacillation is created over the inductor. This voltage is relative to the inductance of the chip-bundle interface and the rate of progress of the current. Thus, when the rationale cells in a circuit are turned on and off, the voltage levels at the power conveyance lines of the circuit change. This inductive commotion is once in a while alluded to as the concurrent exchanging clamor since it is most articulated when an extensive number of I/O drivers switch all the while.

II. PROPOSED METHODOLOGY

In Tri-mode-controlled MTCMOS technique, intermediate PARK mode for ground bounce noise suppression from sleep to active mode a high V_{th} PMOS sleep transistor (called parker) is connected in parallel with the footer as shown in Fig.2.

In dual switch mode system, a middle of the road Hold mode is acquainted to smother the ground bobbing noise, like Tri mode. It is an elective technique to stifle the ground bounce in gated & ground structure as appeared in Fig.3. A high V_{th} NMOS transistor is associated in parallel to the header sleep transistor connected in the middle of genuine power line and virtual power line. Comparatively high V_{th} PMOS transistor is associated in parallel to the footer sleep transistor which is connected in the middle of the genuine ground and the virtual ground line. In a middle of the road hold P2 and N2 high V_{th} transistor turned on and the header (P1) and the footer (N1) are kept up at cut-off mode. In the sleep mode, every one of the transistors i.e sleep transistors (P1, N1) and Parkr transistors (P2, N2) are killed which lessened the sub-edge leakage currents.

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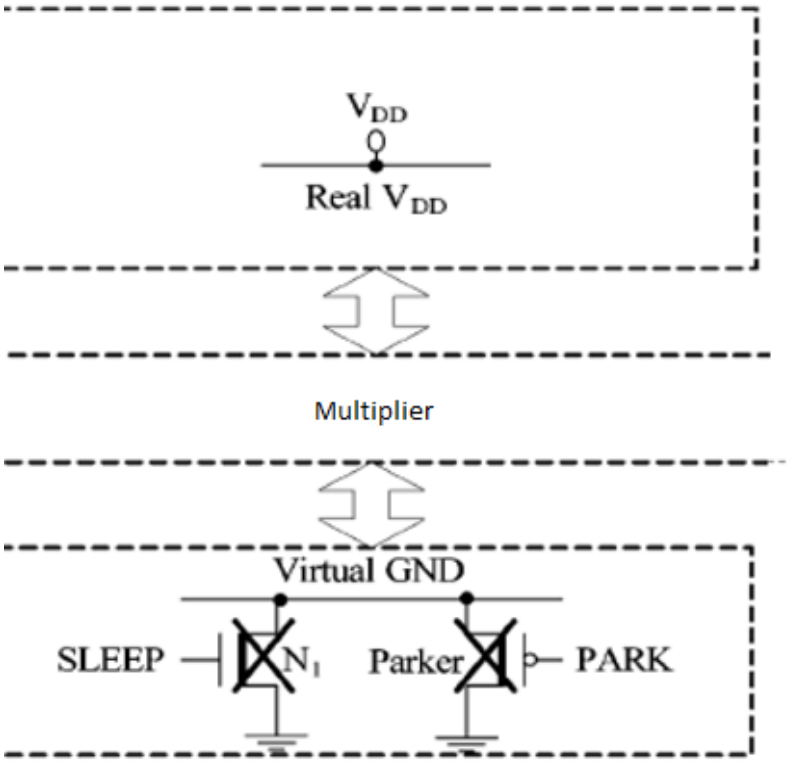

Fig.2 Multiplier with Tri-mode-controlled MTCMOS technique

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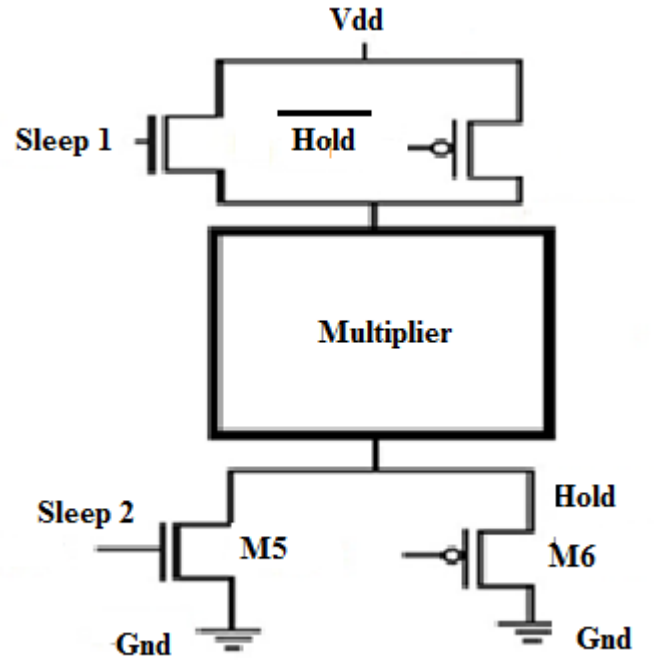

Fig.3Multiplier with dual switch mode MTCMOS technique

The voltages kept up at virtual power and ground lines are roughly equivalent to (Vmid). Prior to the actuation of the circuit, the circuit advances to the middle of the road hold mode i.e from the sleep mode to the hold mode, VDD-Vtn-Vtp voltage is created between the virtual lines. Furthermore, from the hold mode to the active mode change P1 and N1 are enacted. The virtual power line and ground line is charged and released to ~VDD and ~Vgnd. Hold mode diminishes the voltage swing range which lessens the plentifulness of ground skipping noise.

III. SIMULATION AND RESULTS

HSPICE synopsys 2008 software is used to implement the present work. The comparisons of different power gating techniques are shown in Table 1. Ground bounce noise is also shown in Figs. 4-5 for Tri mode power gating technique and Dual switch power gating technique respectively.

Table 1 Comparison of different power gating techniques

Parameter	Base	Tri-Mode	Dual Switch Mode
Average Power (watt)	3.18E-06	1.59E-06	1.64E-06
Leakage Current(A)	7.61E+02	7.53E+02	7.60E+02
Ground Bounce Noise(mV)	-	600	350

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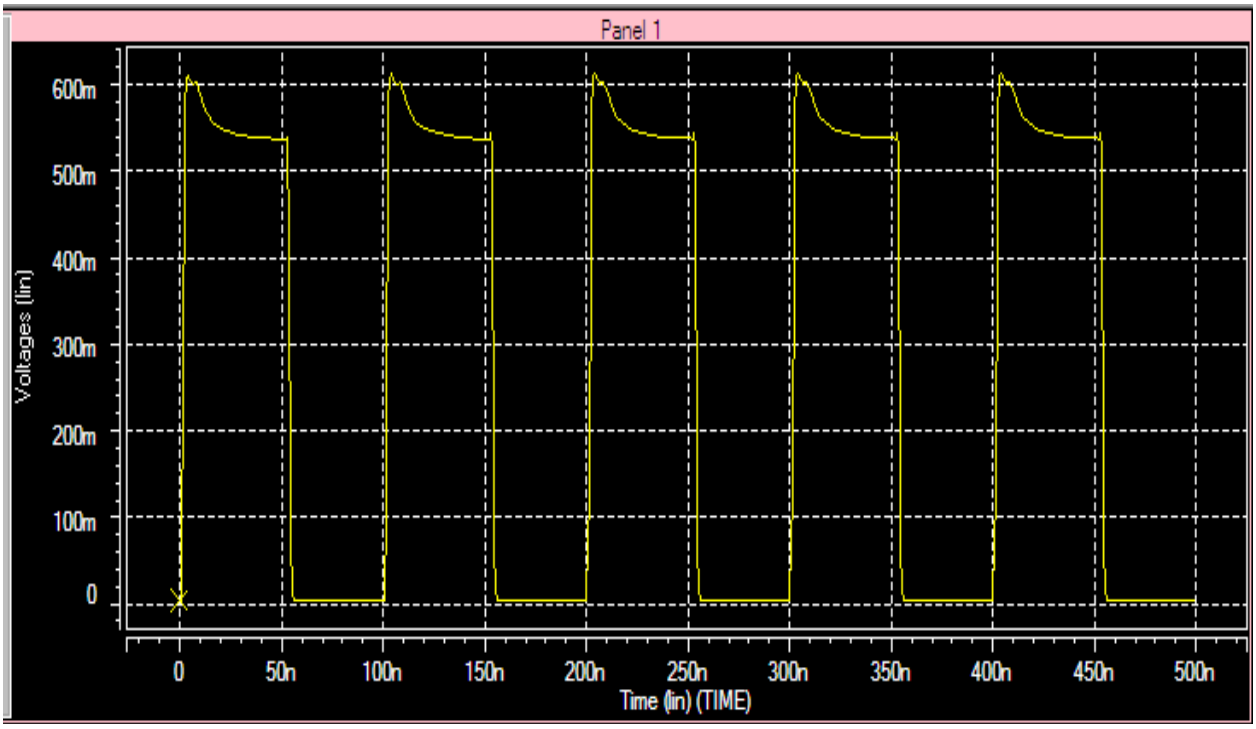

Fig.4 Ground bounce noise with Tri mode power gating technique

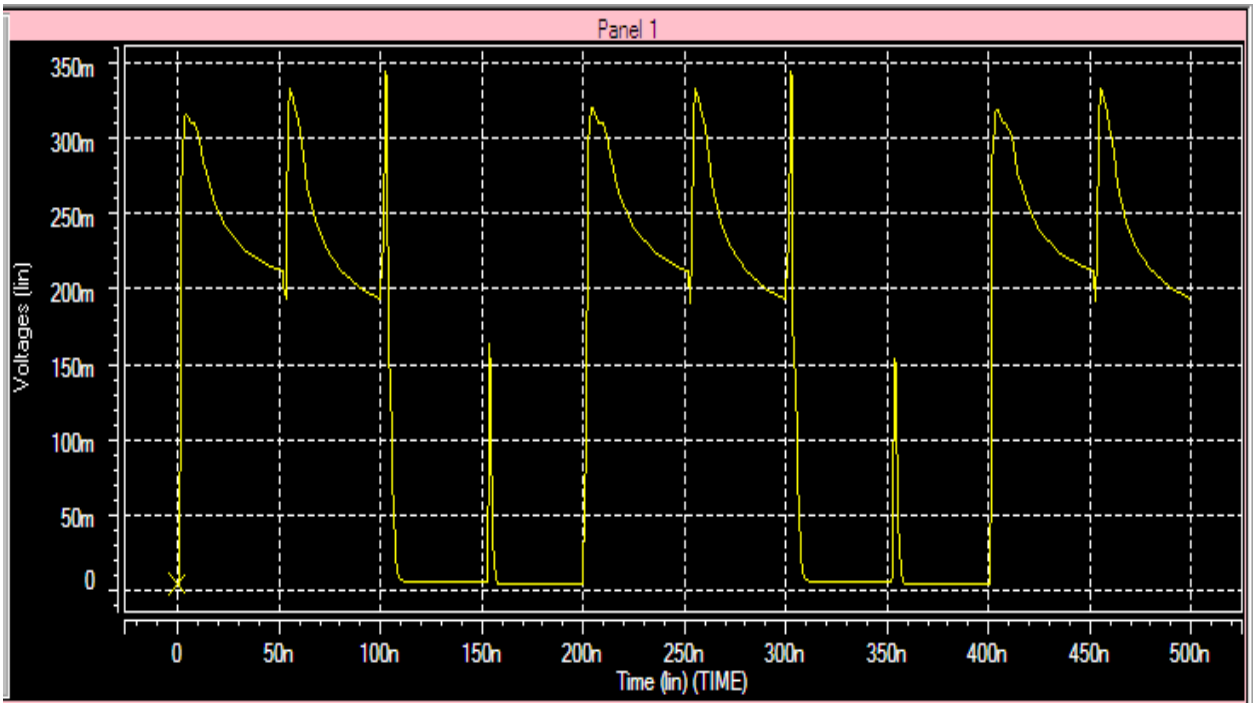

Fig.5Ground bounce noise with Dual switch power gating technique

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IV. CONCLUSION

Proposed dual switch mode technique is best and comparable in terms of leakage current, average power and ground bounce noise with other techniques. Ground bounce noise is reduced 41.66 % in power gating dual switch mode technique compare to tri-mode MTCMOS technique.

V. ACKNOWLEDGEMENT

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